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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,995	08/29/2003	Thomas R. Bednar	BUR920020107US1	1994

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,995	BEDNAR ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-15 and 17-20* is/are rejected.

7)☒ Claim(s) *9 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/29003,10/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/604,995 filed 08/29/2003.

2. Claims 1-20 are pending in the Application.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c).

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed **150 words** in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "the," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

5. Claims 2-9, 11-17, 19 and 20 are objected to because of the following informalities:

claims 4 and 12 are formulated unclear to what Applicant intent to mean, for example, “of said ones”

claim 5 line 3 after “located” delete “alternatingly“ insert –alternatively—

claim 6 line 2 after “wires” delete “are” insert –is--

claim 13 line 3 after “located” delete “alternatingly“ insert –alternatively--

claim 15: dependency of the claim 15 has to be clarified

claim 16 line 2 after “contacts” delete “are” insert –is--

claims 2-9, 11-17, 19 and 20 have insufficient antecedent basis issue

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 10-15 and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuyuki (US Patent 6,404,026).

With respect to claim 1 Tsuyuki teaches an integrated circuit having a plurality of circuits that include at least one I/O circuit and at least one logic circuit within semiconductor device 200 as shown on the Fig. 3 (col. 7, ll.43-47), comprising: a) a contact layer having a plurality of contacts for electrically connecting the integrated circuit to packaging as shown on the Figs. 2, 3 and 5 depicting substrate 11 (col. 5, ll.16-18) including a contact region 40a and 40b (col. 5, ll.34-53); b) a power grid comprising a plurality of metal layers for providing power to the at least one I/O circuit and the at least one logic circuit within a metal wiring layers 19a and 19b and metal wiring layers 20a and 20b as shown on the Figs. 2, 3 and 5 (col. 5, ll.61-67; col. 6, ll.7-13), wherein metal wiring layers 19a, 19b, 20a and 20b are formed from first or second metal wiring layers (col. 6, ll.14-15) and first and second metal layers in the semiconductor device conventionally for power supply and ground; c) a semiconductor device layer in electrical communication with the power grid (col. 5, ll.61-67; col. 6, ll.1-13); and d) a wiring layer interposed between the contact layer and the power grid and electrically connecting the plurality of contacts with the power grid within a fixed potential wiring region 18a and 18b (col. 6, ll.16-21) as shown on the Figs. 2, 3 and 5), wherein the fixed potential wiring layers are disposed between a metal wiring layer (power grid) that is provided with a high potential (voltage) and the element isolation region 14 containing contact regions 40a and 40b with contacts (col. 6, ll.22-31, ll.60-67), the wiring layer including a plurality of wires each having a length extending partly along a first direction and partly along a second direction different from the first direction within the fixed potential wiring layers 18a and 18b having the shape of ring and

extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50).

With respect to claim 10 Tsuyuki teaches an integrated circuit having a plurality of circuits that include at least one I/O circuit and at least one logic circuit circuit within semiconductor device 200 as shown on the Fig. 3 (col. 7, ll.43-47), comprising: a) a contact layer having a plurality of contacts for electrically connecting the integrated circuit to packaging as shown on the Figs. 2, 3 and 5 depicting substrate 11 (col. 5, ll.16-18) including a contact region 40a and 40b (col. 5, ll.34-53); b) a power grid comprising a plurality of metal layers for providing power to the at least one I/O circuit and the at least one logic circuit within a metal wiring layers 19a and 19b and metal wiring layers 20a and 20b as shown on the Figs. 2, 3 and 5 (col. 5, ll.61-67; col. 6, ll.7-13), wherein metal wiring layers 19a, 19b, 20a and 20b are formed from first or second metal wiring layers (col. 6, ll.14-15) and first and second metal layers in the semiconductor device conventionally for power supply and ground; c) a semiconductor device layer in electrical communication with the power grid (col. 5, ll.61-67; col. 6, ll.1-13); and d) a wiring layer interposed between, and electrically connecting together, the contact layer and the power grid within a fixed potential wiring region 18a and 18b (col. 6, ll.16-21) as shown on the Figs. 2, 3 and 5), wherein the fixed potential wiring layers are disposed between a metal wiring layer (power grid) that is provided with a high potential (voltage) and the element isolation region 14 containing contact regions 40a and 40b with contacts (col. 6, ll.22-31, ll.60-67), the wiring layer including a plurality of wires having ring-shaped configurations within the fixed potential wiring layers 18a and

18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50).

Wit respect to claim 18 Tsuyuki teaches a device (col. 2, ll.9-10), comprising: a) a power supply as shown on the Figs. 2, 3 and 5 depicting substrate 11 (col. 5, ll.16-18) including a contact region 40a and 40b (col. 5, ll.34-53); and b) an integrated circuit having at least one I/O circuit and at least one logic circuit within semiconductor device 200 as shown on the Fig. 3 (col. 7, ll.43-47), the integrated circuit comprising: i) a contact layer having a plurality of contacts in electrical communication with the power supply as shown on the Figs. 2, 3 and 5 depicting substrate 11 (col. 5, ll.16-18) including a contact region 40a and 40b (col. 5, ll.34-53); ii) a power grid comprising a plurality of metal layers for providing power to the at least one I/O circuit and the at least one logic circuit within a metal wiring layers 19a and 19b and metal wiring layers 20a and 20b as shown on the Figs. 2, 3 and 5 (col. 5, ll.61-67; col. 6, ll.7-13), wherein metal wiring layers 19a, 19b, 20a and 20b are formed from first or second metal wiring layers (col. 6, ll.14-15) and first and second metal layers in the semiconductor device conventionally for power supply and ground; iii) a semiconductor device layer in electrical communication with the power grid within semiconductor device 200 as shown on the Fig. 3 (col. 7, ll.43-47) and within a metal wiring layers 19a and 19b and metal wiring layers 20a and 20b as shown on the Figs. 2, 3 and 5 (col. 5, ll.61-67; col. 6, ll.7-13), wherein metal wiring layers 19a, 19b, 20a and 20b are formed from first or second metal wiring layers (col. 6, ll.14-15) and first and second metal layers in the semiconductor device conventionally for power supply and ground; and iv) a wiring layer

interposed between the contact layer and the power grid and electrically connecting at least some of the contacts with the power grid within a fixed potential wiring region 18a and 18b (col. 6, ll.16-21) as shown on the Figs. 2, 3 and 5), wherein the fixed potential wiring layers are disposed between a metal wiring layer (power grid) that is provided with a high potential (voltage) and the element isolation region 14 containing contact regions 40a and 40b with contacts (col. 6, ll.22-31, ll.60-67), the wiring layer including a plurality of wires each having a length extending partly along a first direction and partly along a second direction different from the first direction within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50).

With respect to claims 2-8, 11-15, 17, 19 and 20 Tsuyuki teaches:

Claims 2 and 19: each of at least some of the plurality of wires have a ring-shaped configuration within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claims 3 and 11: the ring-shaped configuration is rectangular within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claims 4, 12 and 20: at least some of the ones of the plurality of wires having the ring-shaped configuration are arranged concentrically with one another (col. 9, ll.50-57);

Claims 5 and 13: the plurality of contacts includes a plurality of first contacts and a plurality of second contacts located alternatively with respect to the plurality of first contacts along a plurality of lines, the wiring layer including a plurality of first wires and a plurality of second wires wherein each of the plurality of second wires is laterally spaced from a corresponding one of the plurality of first wires, and each of the plurality of first wires is located on one side of a corresponding one of the plurality of lines and a corresponding one of the plurality of second wires is located on the opposite side of the corresponding one of the plurality of lines within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50);

Claim 6: the plurality of wires is arranged in concentric rings within the semiconductor device having ability of the different configurations of the fixed potential wiring layer (ring) (col. 9, ll.50-57);

Claims 7 and 14: the plurality of wires includes a plurality of Vdd wires and a plurality of ground wires within the fixed potential wiring layers 18a and 18b shown on the Figs, 2, 3 and 5, wherein potentials may be set to a power and ground contacts (col. 4, ll.58-62; col. 6, ll.65-67);

Claims 8 and 15: a plurality of Vddx wires within the fixed potential wiring layers 18a and 18b shown on the Figs, 2, 3 and 5, wherein the fixed potential wiring layers 18a and 18b are fixed at a potential of the semiconductor substrate 11 with desired values (col. 6, ll.60-65);

Claim 17: the power grid comprises a plurality of layers each comprising wires having longitudinal axes all extending in the same direction within the fixed potential wiring layers 18a and 18b having the shape of ring and extending in a rectangular manner, wherein wires can be extended in two different directions (col. 9, ll.48-50), wherein the extension of the wiring direction may be in any configuration (col. 9, ll.50-57).

Allowable Subject Matter

8. Claims 9, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art of record does not teach plurality of contacts is arranged in a square pattern having diagonal symmetry and major axis symmetry.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
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